REMARKS

  The examiner rejected claim 1 under 35 U.S.C. §112, second paragraph as being indefinite.
More specifically, the examiner objects that "one of said input to the finite field multiplier circuit
being the output of the finite field multiplier circuit" appears misdescriptive. We have amended it
in relevant part to read:

> ...of said inputs to the finite field <u>adder</u> ~~multiplier~~ circuit being <u>coupled to</u> the output of the
> finite field multiplier circuit and the other of said inputs to the finite field <u>adder</u> ~~multiplier~~
> circuit being adapted to receive further input

  The basis for the correction is shown in figure 2 and described at paragraph [0056], which
reads "...The output 204 from the finite field multiplier 202 is fed to a finite field adder 206 where
it is combined with the value presented at the third input, C, of the multiply and accumulate cell
200".

  We have also amended claim 1 to positively recite the "at least one field adder circuit"
which was previously recited only indirectly.

  The examiner rejected claims 1-3,5,7, and 9-15 under 35 U.S.C. §102(b) as being anticipated
by US 6,374,383 to Weng.

  The examiner has cited Fig. 2 of Weng against claim 1. Fig. 2 relates to prior art described
in Weng. More specifically, Weng's Fig. 2 is a prior art Chien search circuit. This is confirmed by
Weng at col. 2, lines 46-47.

  One skilled in the art would appreciate that a Chien search is an efficient means of finding
roots of the error location polynomial. All possible potential roots over a Galois field $GF(p^q)$ are
tried until roots for which the error location polynomial has a zero value are identified. Also, a
Chien search assumes that the error locator polynomial is know, whereas finding such a polynomial
is the very subject of our application.

A detailed description is given of the purpose and structure of the Chien search circuit of Fig. 2. The "Chien search circuit 16 includes t+1 multiplier circuits 23" (col. 4, ll 31-32). Each multiplier circuit includes "a register 24 coupled to a Galois Field multiplier 26 for multiplying the contents of the register 24" (col. 4, ll 32-33). Weng contains an error in its description of Fig. 2, when is reads "for multiplying the contents of register 24 by the corresponding power of a and providing feedback into the register 24" (col. 4, ll 33-35). Power of what? In any event, any given multiplier 23 merely multiplies a respective coefficient of the error locator polynomial $\sigma(x)$, which is equation (3) in Weng, by a respective power of a potential root, α, currently under consideration in the Chien search for roots of $\sigma(x)$.

Claim 1 recites "a plurality of arithmetic units". Each of those arithmetic units comprises "a finite field multiplier circuit" and a "finite field adder circuit", which is one basis on which claim 1 distinguishes over Weng. That is, the circuit in Weng comprises an arithmetic unit that performs only finite field multiplications. The circuit 23 in Weng does not have a finite field adder.

The absence of an adder from Weng's circuit 23 means that Weng does not and cannot disclose a coupling between the output of the multiplier circuit and the input of the adder circuit, as required by claim 1.

Even if one skilled in the art considered the XOR gates 30 to be finite field adder circuits, claim 1 recites "one finite field adder circuit for selectively performing at least two finite field arithmetic calculations between values associated with said received code word presented at two inputs to the finite field multiplier circuit and a further value associated with said received code word presented at two inputs to the finite field adder circuit". The multiplier circuit 23 of Weng does not have two inputs, *a fortiori*, it cannot perform a multiplication between values associated with received code words. Therefore, claim 1 further distinguishes over Weng. Indeed, if one skilled in the art was to draw a parallel between adder circuits of Weng and the present application, it appears that the XOR gates 30 of Weng are used to perform a summation function of multiplication results in a manner corresponding to adder circuits 120, 122 and 124 shown in Fig. 1

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of the present application, which calculates the error evaluator polynomial as described at paragraph [0048] of the present application. The latter, in the present application, is recited in the claims by the language "at least one finite field adder circuit for combining respective finite field arithmetic calculation results of respective current finite field arithmetic calculations of at least two of the arithmetic units".
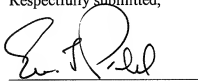
Furthermore, it is to be noted that the system of claim 1 is "for determining at least one of locations and magnitudes of errors in a received code word via respective coefficients of at least part of one of an error-locator polynomial and an error-evaluator polynomial of degree t in at least part of an inversion-free Berlekamp-Massey algorithm, wherein t is an integer". In contrast, the cited Fig. 2 merely concerns finding the roots via a Chien search. It is clear that Fig. 2 of Weng assumes that the error locator polynomial is already known as can be appreciated from, firstly, col. 3, line 66, to col. 4, line 18, and col.. 4, lines 40-42, which read "An additional input to each register 24 is the corresponding coefficient of the error locator polynomial (of Eq. 3) 32"). Therefore, the technical aspects provided by embodiments of the present invention have already been performed in Weng, using "known algorithms, such as the Berlekamp-Massey or Euclidian algorithms" (col. 4, ll 3-4). Hence, embodiments of the present invention and Fig. 2 of Weng are concerned with different aspects of the overall error detection and error correction process.

For at least the reasons stated above, we believe that the claims are in condition for allowance and therefore ask the Examiner to allow them to issue.

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Respectfully submitted,

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